The Surface Detector Trigger for the Auger Observatory

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Abstract

The Pierre Auger Observatory surface array will contain 1600 surface detector stations distributed over 3000 km^2. The large area covered, the limited power budget necessitated by solar power operation, the restricted data bandwidth available through the stations' wireless network connections, and the temperature extremes inherent in an uncontrolled environment, impose special constraints on surface detector trigger system. Several approaches to the implementation of the first level trigger were pursued during the engineering phase of the project in the lab and in the field. In this paper we discuss the solution, based upon industrial grade Altera ACEX® series programmable logic devices, which was chosen for the final design. Trigger algorithms, integration with other aspects of the station electronics, and performance will be described.

1. Introduction

Each surface array station is a water Cherenkov detector [1, 4] which is solar powered, instrumented with low power electronics [8, 4], and communicates with the observatory campus via a custom radio network [3]. Low gain and high gain (32 times larger) signals from three downward facing 9" photomultiplier tubes are sent to the front end electronics, which conditions the signals before digitizing them. Each 25 ns the outputs of six 10-bit analog to digital converters (ADCs) are presented to the trigger/memory circuitry (TMC).

The TMC evaluates ADC outputs for interesting trigger patterns, stores the data in buffer memory, and informs the detector station micro-controller when a trigger occurs. The station controller sends trigger packets, and when requested, event data to the observatory campus via the wireless network. A hierarchical event trigger is used [5, 6] to select events of interest and reject uninteresting events, while keeping within the rate constraints imposed by the station micro-controller, the communications link bandwidth, and the central data acquisition

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system. The TMC generates the first of the hierarchical trigger levels.

2. Design Overview

The design of the TMC utilizes a modular pipelined approach, driven by the same 40 MHz clock as the station micro-controller. The major portions of the design are *triggers, muon buffers, diagnostics,* and *I/O*.

The first level trigger must trigger efficiently on UHE cosmic ray air showers, while simultaneously rejecting most lower energy showers and minimizing composition dependent trigger biases, within a rate constraint of 100 Hz. Note that: 1) On average, for any fixed number of Cherenkov photons detected, those from higher energy showers will be more dispersed in time than those from lower energy showers; and 2) the Cherenkov signals from electrons and photons in the shower are (usually) smaller than those of muons. The level 1 trigger (primarily) uses a low threshold to minimize composition bias, and requires the signals to be extended in time to reject lower energy showers. In order to be fully efficient for a wide range of zenith angle showers and provide sufficient diagnostic and monitoring capabilities, the trigger is actually composed of a number of different sub-triggers. An *external trigger* is the simplest, allowing triggers from an external source. A *random trigger* is useful for measuring background signals without introducing a trigger bias. It is also useful for test purposes. A prerequisite for the other sub-triggers are instances of the *multiplicity trigger*, which are fired whenever a specified minimum number of PMT signals are above respective threshold levels. Alternatively, they can be programmed to fire whenever the sum of a selected set of PMTs is above a *sum threshold*. Several of the *multiplicity triggers* feed *time over threshold* triggers. These implement the primary level 1 trigger algorithm discussed above by requiring that the feeding *multiplicity trigger* module fire a minimum number of times within a sliding window. The required minimum and the window width are adjustable parameters set in registers. Data is accumulated in a circulating shower memory buffer until a trigger occurs. The active buffer is then allowed to continue accumulating data until the trigger position is 1/3 of the way through the buffer. At that point, an interrupt signal is sent to the station controller, the active memory buffer is closed, and a second buffer is made active.

Muon buffers are implemented to: 1) collect a large sample of single muons for calibration and monitoring; and 2) provide information about muons on the edges of an air shower, beyond the set of stations with a shower trigger. They record the ADC signals from the three high gain PMT channels when those signals meet the feeding *multiplicity trigger* instance conditions. This data is zero-suppressed, therefore a time stamp is recorded for each block of data.

The 60 bits of ADC data from the six ADCs are processed by an input module before the data is presented to the remainder of the circuit. This module

buffers the ADC data, or optionally, replaces it with test data from a set of registers, counters, or shift registers.

The TMC interfaces to the station micro-controller bus, an IBM PowerPC 403GCX. The circuit is controlled by programmed data transfer writes/reads to/from registers. Data are transferred from the TMC memory buffers into the station controller memory via direct memory access operations initiated by the station controller.

3. History

The development of the TMC progressed through two parallel paths.

One path that was taken was to develop a custom application specific integrated circuit, using a 0.35μ CMOS process. This effort was successfully carried out through the production of the first prototype iteration of the final design. The prototype chips were demonstrated to be nearly ready for field deployment.

In parallel, a second path was taken utilizing an Altera EP20K200RI240-2 programmable logic device (PLD) and an IDT IDT70V3569S6DRI static RAM chip [9, 10]. This circuit was successfully used in the Auger Engineering Array and demonstrated that the desired functionality could be met with an available commercial PLD. However, this solution far exceeded the cost goals.

We finally adopted a 3rd alternative, utilizing two Altera EP1K100QI2082 PLDs and the IDT memory chip [7, 11], after demonstration of stable operation over a wide temperature range [12]. The cost of this option is a factor of two less than the first PLD approach described above. While still more expensive than the ASIC approach, the reduced technical risk and greater flexibility of a programmable device led us to adopt this solution for production deployment.

See Ref. [13] for a discussion of a possible future option.

4. Final Design

The final design implements double buffered 768 word long, 64 bit wide, shower memory buffers, stored in internal PLD memory. Three *time over threshold* trigger channels are implemented, along with one simple *multiplicity trigger* channel suited for inclined shower triggers. The muon buffers are stored in the external IDT memory. These are also double buffered, with each buffer 8192 32-bit words long.

The PLD code is written in Altera AHDL. The code is heavily pipelined [11] to achieve maximum safety margin in timing. Modern coding practices including modular structure, CVS, and conditional compilation are used to facilitate code reuse, long term maintenance, tracking of code changes, and distribution.

Cadence® Verilog is used to simulate the operation of the three chip TMC. A Verilog model of each of the PLD chips is exported from the Quartus® compiler,

combined with a model of the memory chip obtained from IDT, and incorporated in software test benches that include the worst case timing variations of the microcontroller and ADCs. This has been useful, for example, in identifying timing violations between the PLDs and the memory chip. The Verilog test bench code can optionally generate hardware test vectors. This allows extremely detailed (and automated) timing checks of the actual hardware to be performed [2].

Front end electronics boards containing this TMC, operating with production PLD code, are being installed in the field.

5. Acknowledgments

This work is supported by the US Department of Energy.

6. References

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